Docket No.: 08211/0200348-US0
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Ivan Duzevik et al.

Patent No.: 7,071,739

Issued: July 4, 2006

For: TERMINATION SENSE-AND-MATCH DIFFERENTIAL DRIVER

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.323 AND PATENT OFFICE MISTAKE (37 CFR 1.322)

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted several patent office errors which should be corrected.

The following errors were not in the application as filed by applicant:

In the Application:

Column 3, Line 57, Delete "(lout)" and insert - - (Iout) - -.

Column 4, Line 59, "lout" and insert - - Iout - -.

Column 5, Line 29, Delete "lout" and insert - - Iout - - .

Column 8, Line 2, In Claim 14, after "circuit" insert -- , --.

Column 8, Line 43 (Approx.), In Claim 14, after "transistor" insert -- , --.

Column 10, Line 11, In Claim 19, delete "circuit;" and insert -- circuitry; --.

Column 10, Line 20 (Approx.) In Claim 19, delete "tacks" and insert -- tracks --.

Enclosed please find marked up copies of pages 5, 6 & 7 of the specification, pages 5, 6, 8 & 9 of the claims.

The following errors were found in the application as filed by applicant. The errors now sought to be corrected inadvertent typographical errors, the correction of which does not involve new matter or require reexamination.

Column 5, Line 28, Delete "Bias 1,Bias2" and insert - - Bias 1, Bias 2 - -.

Column 10, Line 29 (Approx.) In Claim 19, delete "op amp" and insert - - operational amplifier - -.

Column 10, Line 32 (Approx.) In Claim 19, delete In Claim 19, delete "op amp" and insert - - operational amplifier - -.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

The Commissioner is authorized to charge any deficiency of up to $300.00 or credit any excess in this fee to Deposit Account No. 04-0100. Payment of $100.00 is enclosed herewith.

Dated: September 20, 2006

Respectfully submitted,

By _____

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	7,071,739
APPLICATION NO.	:	10/755,011
ISSUE DATE	:	July 4, 2006
INVENTOR(S)	:	Ivan Duzevik et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Application:

Column 3, Line 57, Delete "(lout)" and insert - - (Iout) - -.

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and insert - - operational amplifier - -.

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node (N3) and a second feedback node (N4). Resistor Rreplica is coupled in parallel with transistor M14. Operational amplifier circuit A3 is coupled to variable resistance circuit 220A, variable resistance circuit 220B, and transistor M14.

Transistors M0-M3 are arranged to operate as an output signal "switchbox" with differential pair transistors M3 and M2 receiving primary differential phase Vinp and differential pair transistors M1 and M0 receiving inverse differential phase Vinn of signal Vin. The interconnected drain terminals of transistors of M3 and M1 and transistors M0 and M2 substantially contribute to providing the VOD. When transistors M1 and M2 are turned on, transistors M3 and M0 are turned off. Conversely, when transistors M3 and M0 are turned on, transistors M1 and M2 are turned off. Accordingly, an output current (Iout) is steered through resistor Rt to provide the VOD for Vout.

As illustrated in FIGURE 2, the output signal switchbox can be implemented in a complementary arrangement of P-MOSFET and N-MOSFET devices. In another embodiment, the output signal switchbox can be implemented using all P-MOSFET or all N-MOSFET devices.

As illustrated in FIGURE 2, differential input signal Vin may be a dual differential signal. Alternatively, differential input signal Vin may be a single differential input signal with two components. In this case for the complementary arrangement of P- and N-MOSFETs illustrated in FIGURE 2, the gate terminals of transistors M0 and M2 would be driven together by one component of the single differential input signal and the gate terminals of transistors M1 and M2 would be driven together by the other component of this signal.

Variable resistance circuit 220B is a replica of variable resistance circuit 220A. Variable resistance circuit 222B is a replica of variable resistance circuit 222A. Current source circuit 230B is a replica of current source circuit 230A. Current sink circuit 232B is a replica of current sink circuit 232A.

Transistors M6 and M7 are configured as a current source (230A) and a current sink (232A), respectively, for current Iout. Transistor M6 is arranged to be biased by signal Bias1 and transistor M7 is arranged to be biased by signal Bias2 which maintains current Iout in such a manner as to establish and maintain signal Mon at the interconnect between transistors M5 and M6.

Transistor M8 is configured as a current source (230B) that is controlled by signal Bias1. Similarly, transistor M11 is configured as a current sink (232B) that is controlled by signal Bias2. Transistors M10 and M13, with their respective gate terminals biased at power supply rails VSS and VDD, respectively, are biased in their fully on states. Resistor Rreplica and transistor M14 are configured to emulate resistor Rt by providing a total (parallel) resistance that is substantially similar to the termination resistance.

Operational amplifier circuit A3 is configured to provide a third bias signal (Bias3) to modulate transistor M14 such that current source circuit 230A and current source circuit 230B each provide an approximately constant current. Signal bias3 controls, or modulates, an on-resistance of transistor M4. In turn, this controls, or modulates a replica current (Irep) through feedback circuit 204. Further in turn, this controls, or modulates, a monitor replica signal (Monr) at the interconnect of transistors M8 and M9. Operational amplifier circuit A3 is arranged to compare signals Mon and Monr. In one embodiment, signal Mon could appear between transistors M4 and M7 and a corresponding signal Monr could be presented at the interconnect of transistors M11 and M12. Also, operational amplifier circuit A3 could monitor these voltages and provide signal Bias3 in a substantially similar manner.

Operational amplifier circuit A3 is arranged to adjust signal Bias3 to cause signals Mon and Monr to be substantially equivalent. As a result, the drain-to-source voltages Vds, as well as the gate-to-source voltages Vgs (due to signal Bias1), of current source transistors M8 and M6 are also substantially equivalent. Accordingly, the currents Irep and Iout sourced by these transistors M8 and M6, respectively, are maintained at respective values that are determined by the relative sizes (e.g., channel widths) of transistors M8 and M6. For example, if transistors M8 and M6 are of equal size, then currents Irep and current Iout are equal. However, if transistor M6 is larger than transistor M8 by a factor of 10 then the ratio of current Iout to current Irep is Iout:Irep=10:1.

Virtually any scaling factor can be selected, depending upon the desired Irep and Iout currents. Also, depending upon the desired scaling factor, such a scaling factor will be common with respect to the ratios of the sizes of the various transistors as follows:

transistors M8 and M6; transistors M10, M3 and M2; transistors M13, M1 and M0; transistors M11 and M7; transistors M9 and M5; and transistors M12 and M4.

In accordance with this scaling factor, since the transistor stack of output driver circuit 202 and the transistor stack of feedback circuit 204 are substantially equivalent in terms of device count between the power supply rails of VDD and VSS, the respective voltages dropped across these devices will be substantially equivalent. For example, the drain-to-source voltages across transistors M8 and M6 will be substantially equal, as will the drain-to-source voltages across transistors M11 and M7, transistors M10, M3 and M2, and transistors M13, M1 and M0. Additionally, a replica voltage (Vrep) across transistor M14 will be substantially equivalent to the VOD. Also, Vrep can be changed by selection of a first upper reference signal (VREF_UPPER1) and a first lower reference signal (VREF_LOWER2).

Operational amplifier circuit A4 is configured to bias current source circuits 230A and 230B in response to signal VREF_UPPER1 and a first feedback signal (FB1). Operational amplifier circuit A5 is configured to bias current sink circuits 232A and 232B in response to signal VREF_LOWER2 and a second feedback signal (FB2). Operational amplifier circuit A4 is configured to receive and compare signal VREF_UPPER1 and signal FB1 to provide signal Bias1 for transistors M8 and M6. Similarly, operational amplifier circuit A5 is configured to receive and compare signal VREF_LOWER2 and signal FB2 to provide signal Bias2 to transistors M11 and M7. If signal FB1 or FB2 increases (e.g., due to an increase in the replica current Irep) then signal Bias1 or Bias2, respectively, also increases. Conversely, if signals FB1 or FB2 decrease, then the corresponding signal Bias1,Bias2 also decreases. As a result, currents Iout and Irep are maintained at the values necessary to, in turn, maintain the VOD at the value established by the controlling transistor M14.

Variable resistance circuit 220B is configured to vary an associated resistance in response to signal CTL1. Also, variable resistance circuit 222B is configured to vary an associated resistance in response to signal CTL2. Operational amplifier circuit A1 is configured to provide signal CTL1 in response to a third feedback signal (FB3) that is received at node N3 and a second upper reference signal (VREF_UPPER2). Operational amplifier circuit A2 is configured to provide signal CTL2 in response to a fourth

wherein the second operational amplifier circuit is configured to adjust a resistance that is associated with the second variable resistance circuit and a resistance that is associated with the fourth variable resistance circuit.

46. (Currently Amended) The apparatus of Claim 31[[44]],

wherein the output driver circuit further includes a first current source circuit that is coupled to the first variable resistance circuit,

the feedback circuit further includes:

a replica resistor that is coupled in parallel with the transistor;

a second current source circuit that is a replica of the first current source circuit; and

a third operational amplifier circuit that is coupled to the first variable resistance circuit, the third variable resistance circuit, and the transistor, and

wherein the third operational amplifier circuit is configured to adjust the transistor such that the first current source and the second current each provide an approximately constant current.

47. (Canceled)

48. (Canceled)

49. (Currently Amended) A differential driver circuit comprising:

an output driver circuit, including:

differential amplifier circuitry that is configured to provide a differential output signal in response to a differential input signal;

a first variable resistance circuit that is configured to vary a resistance that is associated with the first variable resistance circuit in response to a first control signal; and

a second variable resistance circuit that is configured to vary a resistance that is associated with the second variable resistance circuit in response to a second control signal; and

a feedback circuit that is configured to provide the first control signal and the second control signal, wherein a source resistance of the output driver circuit appears to a load as substantially similar to a termination resistance of the load,

wherein the output driver circuit is further configured to provide a monitor signal,

the feedback circuit includes:

a third variable resistance circuit that is configured to vary a resistance that is associated with the third variable resistance circuit in response to the first control signal,

wherein the third variable resistance circuit is a replica of the first variable resistance circuit;

a fourth variable resistance circuit that is configured to vary a resistance that is associated with the fourth variable resistance circuit in response to the second control signal, wherein

the fourth variable resistance circuit is a replica of the second variable resistance circuit;

a transistor that is coupled between the third variable resistance circuit and the fourth variable resistance circuit;

a first operational amplifier that is configured to provide the first control signal;

a second operational amplifier that is configured to provide the second control signal; and

a third operational amplifier circuit that is coupled to the first variable resistance circuit, the third variable resistance circuit, and the transistor, wherein

the third operational amplifier circuit is configured to modulate the transistor in response to the monitor signal such that the first current source circuit and the second current source circuit each provide approximately constant current~~The differential driver circuit of Claim 48~~,

wherein the output driver circuit further includes:

a first current source circuit that is coupled to the first variable resistance circuit and the feedback circuit; and

a first current sink circuit that is coupled to the second variable resistance circuit and the feedback circuit,

a first variable resistance circuit that is coupled to the differential amplifier circuitry; and

a second variable resistance circuit that is coupled to the differential amplifier circuitry; and

a feedback circuit that is configured to control a resistance that is associated with the first variable resistance circuit and a resistance that is associated with the second variable resistance circuit such that a source resistance of the output driver circuit tracks the termination resistance,

wherein the output driver circuit further includes:

a current source transistor that is arranged to provide a current responsive to a bias signal, wherein the current source transistor operates in a saturation region of operation or an active region of operation, the first variable resistance circuit is coupled between the current source circuit and the differential amplifier circuitry, and wherein the first variable resistance circuit is arranged to receive the current.

55. (Previously Presented) The differential driver circuit of Claim 54, wherein the first variable resistance circuit includes:

a transistor; and

a resistive element that is coupled in parallel with the transistor.

56. (Currently Amended) A differential driver circuit, comprising:

an output driver circuit, including:

differential amplifier circuitry;

a first variable resistance circuit that is coupled to the differential amplifier circuitry; and

a second variable resistance circuit that is coupled to the differential amplifier circuitry; and

a feedback circuit that is configured to control a resistance that is associated with the first variable resistance circuit and a resistance that is associated with the second variable resistance

circuit such that a source resistance of the output driver circuit tracks the termination resistance~~The differential driver circuit of Claim 54~~, wherein

the feedback circuit includes:

a third variable resistance circuit;

a fourth variable resistance circuit;

a transistor that is coupled between the third variable resistance circuit and the fourth variable resistance circuit;

a first op amp circuit that is coupled between the transistor and the third variable resistance circuit; and

a second op amp circuit that is coupled between the transistor and the fourth variable resistance circuit.

57. (Currently Amended) The differential driver circuit of Claim 56[[54]], wherein

the output driver circuit further includes:

a current source transistor that is arranged to provide a current responsive to a bias signal, wherein the current source transistor operates in a saturation region of operation or an active region of operation, the first variable resistance circuit is coupled between the current source circuit and the differential amplifier circuitry, and wherein the first variable resistance circuit is arranged to receive the current.

58. (Previously Presented) The differential driver circuit of Claim 54, wherein

the first variable resistance circuit includes a transistor, the transistor includes a gate, and wherein the feedback circuit is arranged to control the resistance that is associated with the first variable resistance circuit by providing a first control signal to the gate of the transistor such that the transistor is biased in a linear region of operation.

59. (Previously Presented) The differential driver circuit of Claim 58, wherein

the second variable resistance circuit includes another transistor, the other transistor includes a gate, and wherein the feedback circuit is arranged to control the resistance that is associated with